ERA: Embedded Reconfigurable Architecture - past present and future

Computer systems in the last 30 years

- Drastic increase of complexity
- Efficiency is not increasing
- Understanding is decreasing
- No reliability anymore
- Waste of power consumption
- Inefficient use of parallelism
- Applicability not achieving its potential

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ERA: Embedded Reconfigurable Architecture

Fundamental redesign required

- Programming language
  - Simple, natural and practical model
  - Machine-independent concept
- Runtime system
  - Simple design and clean implementation
  - Configurable (redundancy, parallelism, power)
- Computer machine
  - Simple, efficient, parallel, small and embedded
  - Reliability with configurable redundancy

ERA: Embedded Reconfigurable Architecture

Consortium

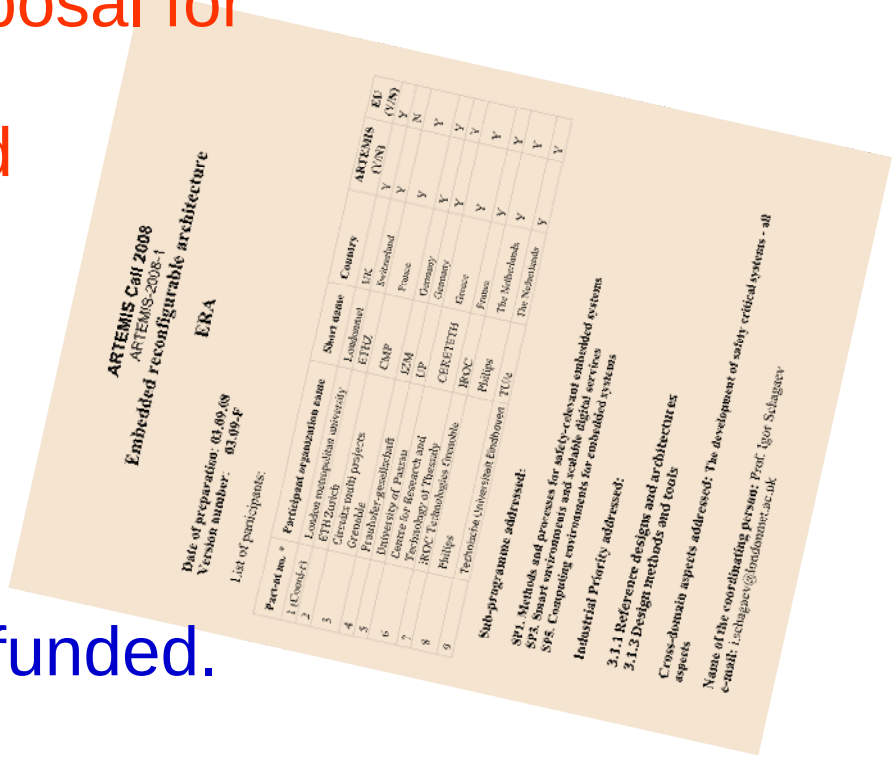
- London Metropolitan University (UK) — SW
- ETH Zürich (Switzerland)
- Centre of RT Thessaly (Greece)
- Fraunhofer-Gesellschaft (Germany)
- Circuits Multi Projects (France) — HW
- Cambridge Technology Group (UK)
- Phillips (The Netherlands)
- TU Eindhoven (The Netherlands)

App

ERA: History and progress

Actions

- Londonmet submitted proposal for Artemis call 2008
- Proposal passed threshold
- TSB did support ERA
- BERR did support ERA



ARTEMIS Call 2008
ARTEMIS-2008-1
Embedded reconfigurable architecture
ERA

Date of preparation: 03.09.08
Version number: 03.09-F
List of participants:

Part.nr.	Participant organization name	Short name	Country	ARTEMIS (Y/N)	EU (Y/N)
1 (Coord.)	London metropolitan university	Londonmet	UK	Y	Y
2	ETH Zurich	ETHZ	Switzerland	Y	Y
3	Grenoble	CMP	France	Y	N
4	Fraunhofer gesellschaft	IZM	Germany	Y	Y
5	University of Patras	UP	Greece	Y	Y
6	Centre for Research and Technology of Thessaly	CERETETH	Greece	Y	Y
7	SOC Technologies Ensemble	BSOC	France	Y	Y
8	Philips	Philips	The Netherlands	Y	Y
9	Technische Universiteit Eindhoven	TU/e	The Netherlands	Y	Y

Sub-programme addressed:
SP1. Methods and processes for safe(r)-relevant embedded systems
SP3. Smart environments and scalable digital services
SP5. Computing environments for embedded systems

Industrial Priority addressed:
3.1.1 Reference designs and architectures
3.1.3 Design methods and tools

Cross-domain aspects addressed: The development of safety critical systems - all aspects

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- In spite of it ERA was not funded.

ERA now: principles

Simplicity ERA avoids introducing extra hardware and software ‘bells and whistles’ in the architecture to placate history (compatibility with main market players) or conventions (pipelines, caches etc)

Redundancy Deliberate introduction of hardware and system software redundancy together with monitoring schemes provides ERA reconfigurability, used for performance or reliability. Redundancy is used for the implementation of three processes: checking, recovery preparation and recovery

Reconfigurability ERA reconfigurability has three main purposes: performance, reliability and power awareness. Handling reconfigurability using GLL and run-time support provides unique flexibility for ERA in implementation of the required reliability or performance ratio and monitoring, if necessary graceful degradation

Scalability Active support of reconfiguration is managed in real time by controlling hardware and system software resources. The software and hardware are both specifically designed to scale up to hundreds of processors.

Reliability FT Minimum HW redundancy is used in the design of highly reliable main ERA components. This eases combining them together and reducing complexity of the required connections. Redundancy of HW and SSW deliberately introduced and managed to maximize both: tolerance of malfunctions and permanent faults. The SSW performs HW monitoring in terms of fault tolerance.

Resource-awareness Mission critical systems as well as everyday applications may have significant limitations, in terms of hardware resources (computational and memory) and power consumption constraints, (e.g. battery life). Thus reconfigurability as a new feature must be exploited through hardware-software co-design to be resource-wise.

ERA: implementation 2010

- **Theoretically:** new paradigm of reconfigurable computing was proposed and developed, including two key models Graph Logic model and Control-Data-Predicate model
- **In system software:** new language for scalable computing is proposed and compiler for ERA processing element developed (using simulator)
- **In system software:** Structure of run-time system for reconfigurable architecture is developed
- **In hardware:** processor simulator is developed
- **In hardware:** processor designed (Altera based)
- **In hardware:** performance and reliability modeling exist

ERA: 2010 Hardware results, ctd

- Complexity comparison:
  - ERRIC / Intel Itanium (Merced)
  = 1/30000
  - ERRIC / ARM7TDMI
  = 1/10
- It means that i-phone battery powered and similar size ERA is faster than graphic heavy desktop station

Execution Time Comparisons

80x86 22* 2L+20*1L+16*1L +12*2L +8*1L +6*1L +5*1L +4*1L +2*1L

EURRICA 22* L+20*1L+(16*1L +12*2L +8*1L +6*1L +5*1L +4*1L)/2 +2*1L

= 1.66

[SPECint92, Hennessay and Patterson 2001]

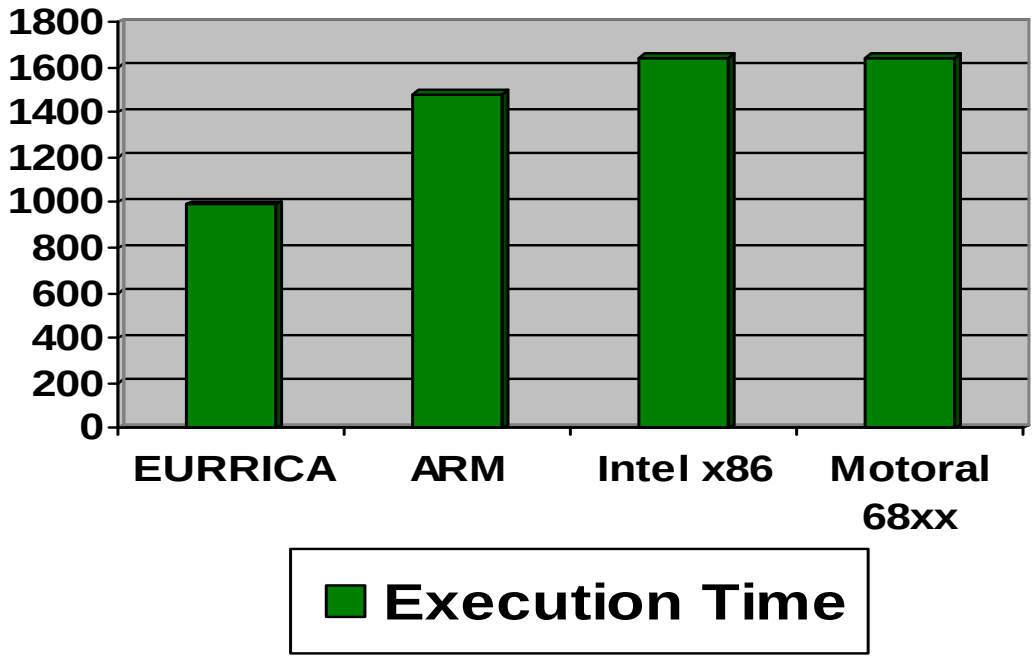
ARM 26* 2L+19*1L+12*1L +10*2L +9*1L +5*1L +4*1L +6*1L +8*1L

EURRICA 26* L +(19*1L +36L +10*2L +18*1L +6*1L)/2 +5*1L

= 1.67

[SPECint2000, Hennessay and Patterson 2001]

ERA: 2010 Hardware results



The execution time in nanoseconds
(assuming the memory used are 100MHz SDRAMs)

ERA: 2010 Hardware results

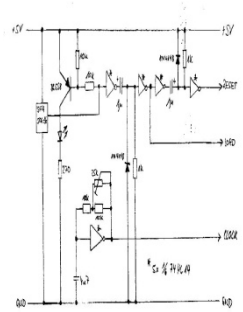
- **Reliability:**
  - ERA is the first fault tolerant processor with fault tolerance achieved at the level of instruction
  - ERA has 12% of deliberately introduced redundancy to gain 5.9 times higher reliability
  - ERA is malfunction tolerant architecture with explicit separation of types of hardware faults

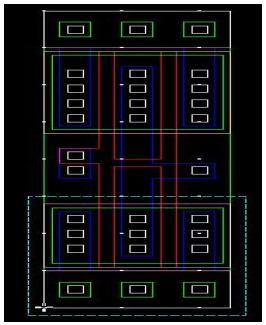
ERA: 2010 Hardware results

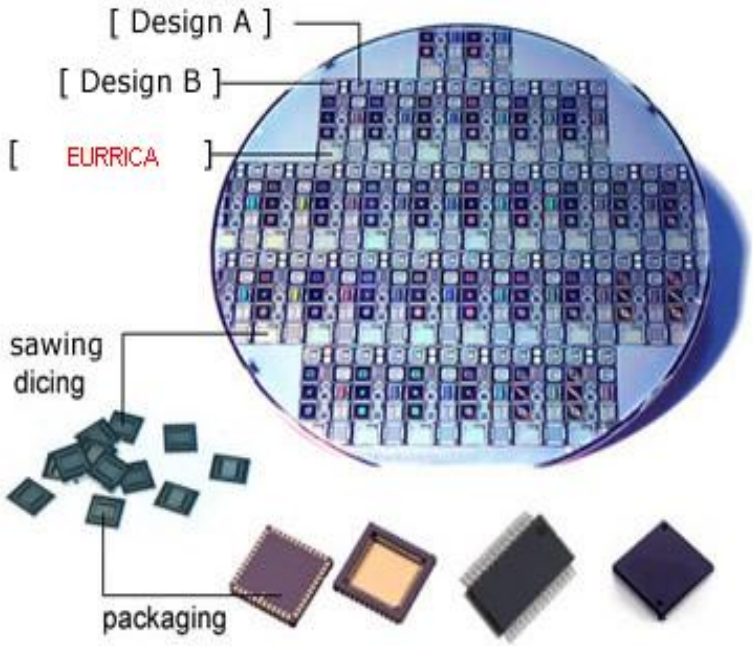
- How it looks today:

Future Plans

- Logic Validation and Testing Using Altera FPGA Devices
- Mapping Logic Design to Circuit Design
- Circuit Design to Layout
- Manufacturing
- Silicon Debug and Test







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