The following table compares an existing industrial vision, the highly promoted Leon, with a proposed architecture in ERA. Main parameters and design solutions are compared with detailed reasoning why ERA must be designed and developed instead of industrially dominant components.

Hardware Industrial vision (Leon) vs. ERA proposal

Industrial State of the Art (Leon3FT)	Proposed by ERA	Comment
SPARC V8 instruction set with V8 extensions	New, compact and efficient instruction set with ability to control / repeat.	ERA instructions are checkable and repeatable; no fault propagation beyond one instruction execution.
Pipelining – 7 stages	NO pipelining.	Fault tolerance is UNACHIEVEABLE with pipelining at the instruction level.
Memory management - Cache for instructions; - Cache for data.	NO cache as instructions are ½ word and performance is adequate, without need of smoothing processor / memory differences.	In ERA there is NO need for synchronization schemes and assumptions about various types/timing of faults, as cache memory does not exist.
Fault tolerance: - Single event fault (SEU) up to 4 errors per 32bit words; - Memory ECC; - Data mirrored in a secondary memory (cache).	Malfunction tolerance for any power of fault (up 16 bits) at the chip level. Fault tolerance for permanent faults at the architecture configuration level (processor / memory and integration (T-logic))	ERA implemented on a chip using the same assumption about power of fault with adjustment of checking and recovery schemes within single instruction. Consistent use of the same technology.
Fault tolerance technology Radiation tolerance tests	Deliberate design with topologic support of FT.	ERA tolerates malfunctions and permanent faults.
Supportive library C++	ERA new language - derivative from Oberon maximum efficiency HW and SW resources use at run-time level.	EU made, maximize both: reliability of software design and hardware performance and reliability.
OS Linux support	ERA proposes new OS for embedded reconfigurable OS (EROS) with full support of malfunction and permanent fault tolerance of hardware.	EU made, patentable, exceptionally reliable with rigorously defined features and functions.
Hardware debug support Debug mode with interfaces PCI Ethernet JTAG USB RS232	Identical, plus new FT interface.	For embedded systems of safety critical applications ERA is developing new reliable interface; existing interfaces are supported mostly for debugging purposes.
Technologies ASIC	Technology ASIC	ERA will be implemented on wafer.
Evaluation board exists.	Evaluation board exists Software simulator – exists (except FT mode)	