Power of a theory is in it's predictions and ability to apply them

HW RESULTS

November 2009 Issue No 1109 www.it-acs.co.uk

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Device & results chronology

Von Neumann was not always right: design of reliable system is better to do with reliable components

RELIABLE DESIGN FROM RELIABLE COMPONENT

FAULT TOLERANT AVIONICS

Active safety system for aircraft with double Motorola 68020, fault tolerant memory for applications (41 chip of SRAM) and new tripled memory together with flight data recorder with unique thermo-resistant system - were developed and tested.

Completed 1994

ERRIC

Embedded recoverable reduced instruction computer was designed and prototyped in 1998-2008 before and within FP6 ONBASS project (www.onbass.org). Malfunction tolerance and rigorous design enabled to achieve fault tolerance with 12% structural redundancy and zero time redundancy. ERRIC requires 6.5 times less power than ARM and has similar performance.

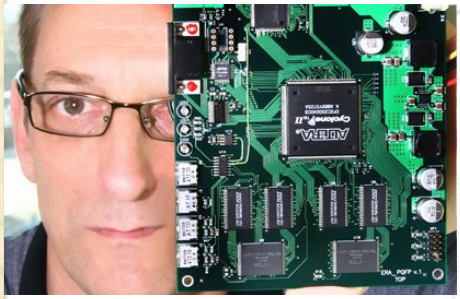
1998-up to now

NEXT STOP - NEW ERA

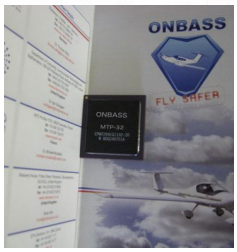
Idea to combine ERRIC and our memory designs to make fault tolerant reconfigurable architecture on a wafer became known as ERA (evolving reconfigurable architecture).

In progress

from left to right: new triple memory, active flight control system, flight data recorder all 1994



fault tolerant computer ERRIC2009



32bit fault tolerant processor 2007

Triplicated memory (TRAM) - right picture was developed in 1992. Malfunction tolerance of the device is unique.